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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/466,665	12/20/1999	JAMES MOSER	9-13528-82US	1452

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EXAMINER	
ODOM, CURTIS B	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 02/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/466,665	Applicant(s) MOSER ET AL.	
	Examiner Curtis B. Odom	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/20/99* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,32-35,67 and 68* is/are rejected.

7)☒ Claim(s) *6-31, 36-66, and 69-78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *12/20/99* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 32 is objected to because of the following informalities: The word "course" is suggested to be changed to "coarse". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5 and 67-68 are rejected under 35 U.S.C. 102(b) as being anticipated by Buchwald (U. S. Patent No. 5, 757, 857).

Regarding claim 1, Buchwald discloses a digital frequency detector (Fig. 4, column 6, lines 18-20) for detecting a difference between a frequency of an oscillator output signal and a frequency of a data signal (column 7, lines 12-17), the digital frequency detector comprising:

first digital sample means (Fig. 4, column 3, lines 57-60) for sampling the oscillator output signal at a timing of the data signal to generate a first beat signal.

second digital sample means (Fig. 4, column 3, lines 57-60) for sampling a quadrature clock signal at a timing of the data signal to generate a second beat signal.

third digital sample means (Fig. 4, column 3, lines 62-67, column 4, lines 1-14 and 66-67, and column 5, lines 1-10) for sampling the second beat signal at a timing of the first beat signal to generate a frequency error.

Regarding claim 2, Buchwald discloses a digital frequency detector as claimed in claim 1, wherein a frequency of the quadrature clock signal is substantially identical to that of the oscillator output signal, and a phase difference between the quadrature clock signal and the oscillator output signal is between 45 and 135 degrees (column 10, lines 55-63), wherein if the output of the oscillator is a quadrature clock signal, the quadrature clock signal and the output of the oscillator have the same frequency.

Regarding claim 3, Buchwald discloses a digital frequency detector as claimed in claim 2, wherein a phase difference between the qudrature clock signal and the oscillator output signal is about 90 degrees (column 10, lines 55-58).

Regarding claim 4, Buchwald discloses a digital frequency detector as claimed in claim 1, wherein the first sample means comprises:

a first pair of digital latch circuits respectively adapted to sample the oscillator output signal on rising and falling edges of the data signal (Fig. 4, blocks 64 and 66); and

a first multiplexor adapted to selectively switch between respective outputs of the first pair of digital latch circuits on transitions of the data signal (Fig. 4, block 72).

Regarding claim 5, Buchwald discloses a digital frequency detector as claimed in claim 1, wherein the second sample means comprises:

a second pair of digital latch circuits respectively adapted to sample the quadrature clock signal on rising and falling edges of the data signal (Fig. 4, blocks 68 and 70); and

a second multiplexor adapted to selectively switch between respective outputs of the second pair of digital latch circuits on transitions of the data signal (Fig. 4, block 72).

Regarding claim 67, Buchwald discloses a method recovering a clock signal from a received data signal, comprising the steps of:

sampling (Fig. 4, column, 3, lines 54-67) the received data signal using a phase detector that generates a phase error signal indicative of a detected phase difference between the data signal and an oscillator output signal, and a digital frequency detector (Fig. 4, column 4, lines 66-67, and column 5, lines 1-16 and 36-41)

selecting (Fig. 4, lock detect gate, column 5, lines 11-16 and column 16, lines 31-39) an output of the phase detector when the detected frequency difference is small and otherwise selecting the output of the digital frequency detector to generate the recovered clock signal, wherein the value of the absolute phase error detects large frequency differences; and

using the selected one of the outputs of the phase detector and the digital frequency detector to control an oscillator to generate the recovered clock signal (column 5, lines 11-16, column 16,)

Regarding claim 68, Buchwald discloses a method as claimed in claim 67, wherein selecting an output of the phase detector and the digital frequency detector is performed by a control unit (Fig. 4, lock detect gate, column 5, lines 11-16 and column 16, lines 31-39), wherein the lock detector gate acts is a control unit.

4. Claims 32-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyashita et al. (U.S. Patent No. 5, 889, 828).

Regarding claim 32, Miyashita et al. discloses a system for recovering a clock signal from a data signal, comprising:

an oscillator (Fig. 6, block 961, column 12, lines 48-60) adapted to generate an oscillator output signal;

first detecting means (Fig. 6, block 964, column 12, lines 48-51) for obtaining a coarse frequency-lock condition between the data signal and a recovered clock signal;

second detecting means (Fig. 6, block 966, column 12, lines 55-58) for obtaining a phase-locked condition between the data signal and the recovered clock signal;

lock-detecting means (Fig. 6, block 969, column 13, lines 3-10) responsive to the first detecting means for detecting an out-of-lock condition between the data signal and the recovered clock signal; and

control means (Fig. 6, block 969, column 13, lines 3-10 and 20-25) responsive to the lock-detecting means and adapted to control the oscillator to generate an oscillator output signal on the basis of the first detecting means during an out-of-lock condition, and otherwise to generated the oscillator output signal on the basis of the second detecting means.

Regarding claim 33, Miyashita et al. discloses a system as claimed in claim 32, wherein the second detecting means comprised a phase detector adapted to generate a phase error signal indicative of a detected phase difference between the data signal and the oscillator output signal (Fig. 7, block 20, column 13, lines 51-67, and column 14, lines 1-19).

Regarding claim 34, Miyashita et al. discloses a system as claimed in claim 32, wherein the first detecting means comprises a digital frequency detector adapted to generate a frequency

error signal indicative of a detected frequency difference between the data signal and the oscillator output signal (Fig. 7, block 40, column 2 lines 61-66, and column 14, lines 40-44).

Regarding claim 35, Miyashita et al. discloses a system as claimed in claim 34, wherein the lock-detecting means comprises a frequency lock detector responsive to the digital frequency detector and adapted to generate a lock-indicator signal indicative of a frequency-lock condition between the data signal and the oscillator output (Fig. 63, block 31, column 42, lines 40-43).

Allowable Subject Matter

5. Claims 6-31, 36-66, and 69-78 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 703-305-4097. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Curtis Odom
January 29, 2003

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600